

VPU PRODUCT BRIEF

Movidius provides the ultimate in low-power vision processing solutions, which include the **Myriad 2 family of vision processing units (VPUs)** plus a comprehensive **Myriad Development Kit (MDK)**, a reference hardware EVM and optional Machine Vision Application Packages.

The Myriad 2 MA2x5x family of system-on-a-chip (SoC) devices offers significant computation performance and image processing capability with a low-power footprint. The Myriad 2 lineup includes the following product configurations:

MA2150: 1 Gbit DDR

MA2155: 1 Gbit DDR and secure boot

MA2450: 4 Gbit DDR

MA2455: 4 Gbit DDR and secure boot

Myriad 2 VPUs offer TeraFLOPS (trillions of floating-point operations per second) of performance within a nominal 1 Watt power envelope. The Myriad 2 architecture includes enough performance to support multiple cameras with flexible image signal processing pipelines for each camera, and software programmable vision processing with fixed- and floating-point datatypes supported. A robust overall dataflow design ensures mitigation of processing bottlenecks.

FLEXIBLE COMBINATION OF MACHINE VISION WITH ISP

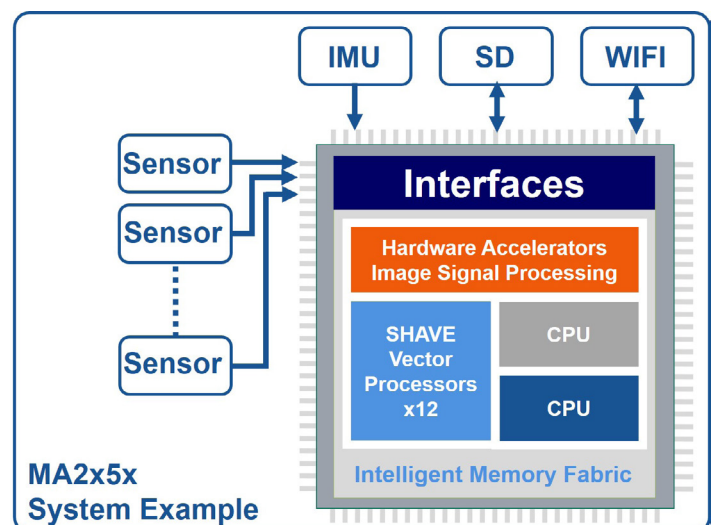
Myriad 2 MA2x5x incorporates an innovative approach to combine image signal processing with vision processing. A set of imaging/vision hardware accelerators supports a world-class ISP pipeline without any roundtrips to memory; at the same time they are repurposed to accelerate developers' vision processing algorithms in conjunction with a set of special purpose VLIW vision processor cores. All processing elements are tied together with a multi-ported memory that enables implementation of demanding applications with high efficiency.

TARGET APPLICATIONS

- Deep Neural Network-based Classification
- Pose Estimation
- 3D Depth
- Visual Inertial Odometry (Navigation)
- Gesture/Eye Tracking and Recognition

EXAMPLE PRODUCT CATEGORIES

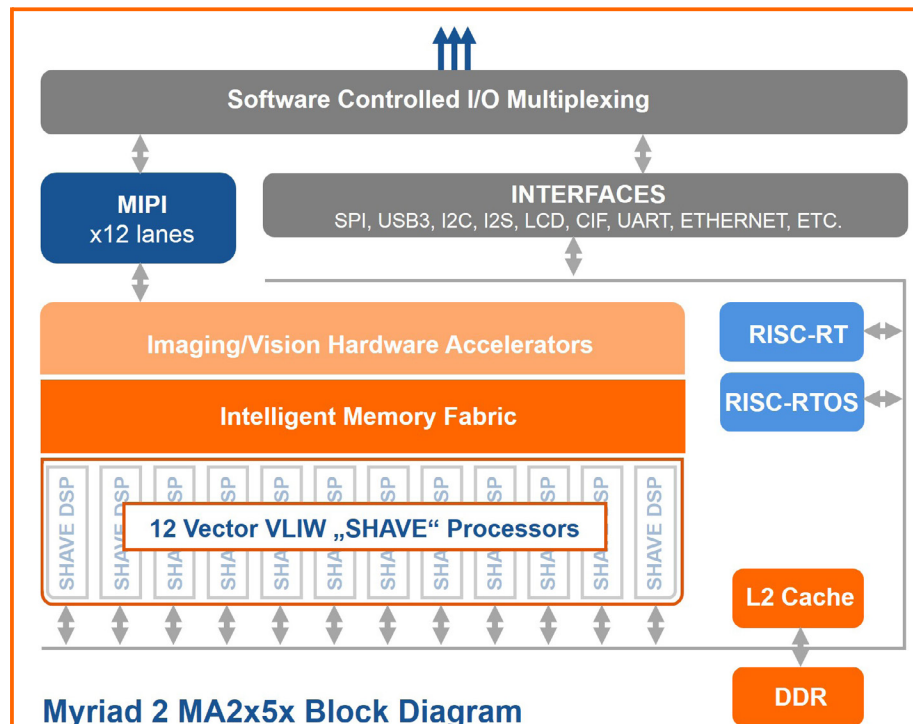
- AR/VR Head Mounted Displays (HMDs)
- Drones/UAVs
- Security/Surveillance Cameras
- Service Robotics



See the **MDK Product Brief** for an overview of the robust Myriad Development Kit, including the software development frameworks, tools, drivers, and libraries, to enable developers to implement applications on Movidius VPUs.

MYRIAD 2 SoC SPECIFICATIONS

- **Heterogeneous, high throughput, multi-core architecture based on**
 - 12 VLIW 128-bit vector SHAVE Processors optimized for machine vision
 - Configurable hardware accelerators for image and vision processing, with line-buffers enabling zero local memory access ISP mode
 - **Support for 16/32-bit floating point and 8/16/32-bit integer operations**
 - **Homogeneous, centralized memory architecture; 2MB of on-chip memory**
 - **400 GB/sec of sustained internal memory bandwidth**
 - **256 KB of L2 Cache**
 - **Power management: 20 power islands; low power states**
 - **Nominal 600 MHz operation at 0.9 V**
 - **Rich set of interfaces:**
 - 12 Lanes MIPI, 1.5 Gbps per lane configurable as CSI-2 or DSI
 - I2C, SPI for control and configuration
 - I2S for audio input
 - Banks of configurable GPIO, PWM
 - **Available package configurations**
 - MA2150/MA2155:
6.5mm x 6.5mm
0.4mm pitch,
225 Ball BGA
1Gb LPDDR II
 - MA2450/MA2455:
8mm x 9.5mm
0.5mm pitch
270 Ball BGA,
4Gb LPDDR III
 - **Advanced low-power 28nm HPC process node**
- 2 x 32-bit RISC processors
 - Supports data and task parallelism
 - Programmable Interconnect
 - USB3 with integrated PHY
 - 2-Slot SDIO
 - Debug interface
 - 1 Gbit Ethernet



Myriad 2 MA2x5x Block Diagram